IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of: **Wu et al.**	)	
MMB Docket No. **1890-0246**	)	Examiner: **To be assigned**
Application No. **10/537,029**	)	Group Art Unit: **To be assigned**
Filed: **May 31, 2005**	)	
For: **Current-Controlled Oscillator**	)	

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

October 20, 2005
(Date of deposit)

James D. Wood
Name of person mailing Document or fee

Signature

October 20, 2005
Date of Signature

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, Applicants hereby disclose the following reference(s) regarding the above-identified patent application.

U.S. Patent No.	Inventor	Issue Date
5,799,051	Leung et al.	Aug. 25, 1998
5,600,280	Zhang	Feb. 4, 1997
5,206,609	Mijuskovic	Apr. 27, 1993

Articles

1) Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, Nov. 1996, pp. 1723-1732, (10 pages).

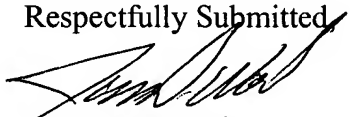
2) Chan et al., "A 622-MHz Interpolating Ring VCO with Temperature Compensation and Jitter Analysis", IEEE International Symposium on Circuits and Systems, Jun. 1997, Hong Kong, pp. 25-28, (4 pages).

U.S. Patent Nos. 5,799,051, 5,600,280 and 5,206,609 were cited in an International Search Report (copy enclosed) dated Feb. 17, 2003 for priority application PCT/SG02/00283 filed Nov. 29, 2002.

Pursuant to 37 C.F.R. § 1.97(b), this Information Disclosure Statement is being filed within three months after the filing date of the application or before the mailing of the first office action on the merits.

It is believed that no fees are due for the consideration of this Information Disclosure Statement. However, the Commissioner is hereby authorized to charge any deficiency or to credit any overpayment to Deposit Account No. 13-0014, but not to include any payment of issue fees.

Respectfully Submitted,



James D. Wood
Attorney for Applicants
Registration No. 43,285

October 20, 2005

Maginot, Moore & Beck
Bank One Center Tower
111 Monument Circle, Suite 3000
Indianapolis, Indiana 46204-5115
(317) 638-2922 phone
(317) 638-2139 fax

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	MMB DOCKET NO. 1890-0246	APPLICATION NO.: 10/537,029
	APPLICANT(S): Wu et al.	
	FILING DATE: May 31, 2005	GROUP ART UNIT: TBD

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA	5,799,051	Aug. 25, 1998	Leung et al.			
	AB	5,600,280	Feb. 4, 1997	Zhang			
	AC	5,206,609	Apr. 27, 1993	Mijuskovic			
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL						Yes No
	AM						Yes No
	AN						Yes No
	AO						Yes No
	AP						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AQ		Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, Nov. 1996, pp. 1723-1732, (10 pages).
	AR		Chan et al., "A 622-MHz Interpolating Ring VCO with Temperature Compensation and Jitter Analysis", IEEE International Symposium on Circuits and Systems, Jun. 1997, Hong Kong, pp. 25-28, (4 pages).
	AS		

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicants.